AMENDMENTS

Please amend the application as follows:

In the Specification:

Please amend the paragraph starting on page 10, line 23, as follows:

Any of the other stages 25, 32, and/or 35 that may produce predicate data are similarly coupled to the register file 71, so that the register file 71 may receive and appropriately process the predicate data. For example, the detect exceptions stage 32 in FIG. 2 is coupled to the register file 71 such that the processing circuitry 62 may transmit a new predicate data bit produced in processing circuitry 62 to the register file 71 via latch 83 and connections 85 and 86. Furthermore, the register identifier identifying the register 73 (FIG. 3) where the new predicate bit should be written may be transmitted to register file 71 via latch 83 and connections 86 and 87 ~~and 88~~. Although not shown by FIG. 2, any of the stages 25, 28, 32, and/or 35 of any other pipeline 21 may be similarly coupled to the register file 71 so that the register file 71 may receive predicate data from the stages 25, 28, 32 and/or 35 of other pipelines 21.

Please amend the paragraph starting on page 22, line 4, as follows:

The latch 172 transmits QP_{exe} to OR gate 106 via connection 155 upon the next active edge of a clock signal. This should be the same active edge upon which the instruction in the register stage 25 enters the execution stage 28. The OR gate 106 also receives a pessimistic control signal from predicate control circuitry 143. The pessimistic control signal is asserted when the predicate control circuitry 143 detects that an instruction in any of the pipelines 21 may produce predicate data that may later affect the predicate status of the instruction presently in the execution stage 28. Therefore, similar to the output by OR gate 98, the output of OR gate 106 is asserted, if the predicate value from latch 172 indicates that the instruction in the execution stage 28 is enabled (*i.e.*, if the predicate value from latch 172 is asserted in the preferred embodiment) or if the pessimistic control signal from predicate control circuitry 143 is asserted. If the output of OR gate 106 is asserted, the processing circuitry 56 is then designed to process the instruction in the execution stage 56 as if the instruction is enabled. Conversely, if the output of OR gate 106 is deasserted, then the processing circuitry 56 is designed to process the instruction in the processing circuitry 56 as if the instruction is disabled.